

**Description****Analog-to-digital converter**

5 The invention relates to an analog-to-digital converter.

An analog-to-digital converter (ADC) is an electronic circuit or an electronic chip which converts an analog signal into a digital equivalent. An ADC converts a continuous-value voltage value into a binary number which indicates how often a particular voltage range is included within the voltage value.

15 Analog-to-digital converters (ADCs) are used at interfaces between analog signals and digital data processing. Fundamental service features of an ADC are the achievable resolution of the converter (measured in bits) and the conversion speed (measured in samples per second: Sa/s). Particularly in the field of communications engineering, there is a need for very fast converters, i.e. converters with high conversion rates (e.g. >1 GSa/s). The resolution of known converters is normally between 5 bits and 8 bits, and 20 25 the circuit architecture is based on a flash converter architecture.

Figure 1 shows an analog-to-digital converter 100 which is known from the prior art.

30 The analog-to-digital converter 100 has a multiplicity of comparators 101 which each have a first input 102, a second input 103 and an output 104. Provided at the first input 102 of each comparator is a signal 108  $V_{in}$  for digitization in the form of an electrical voltage signal. Connected between a respective second input 103 on a comparator 101 and a positive reference potential 35 106  $V_{ref+}$  or a negative reference potential  $V_{ref-}$  is a

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number of nonreactive resistors 105 which is characteristic of each of the comparators. By way of example, a single resistor 105 is connected between the second input 103 of the top comparator 101 in figure 1 and the positive reference potential 106, two nonreactive resistors 105 are connected between the second input 103 of the second-from-top comparator 101 in figure 1 and the positive reference potential 106  $V_{ref+}$ , etc. Clearly, the voltage drop across the nonreactive resistors 105 connected between the reference potential 106, 107 and the second input 103 of a respective comparator 101 is used to reduce the potential applied to the second input 103 in figure 1 from the top to the bottom in stages, so that a comparative result at the outputs of the comparators 101 supplies a sequence of output values with the logic value "1" and then a sequence of output values with the logic value "0". This digitized output signal is called a thermometer code, where the number of comparator outputs 104 providing a logic value "1" represents a digitized measure of the value of the signal 108 for digitization.

In the case of the circuit shown in figure 1 for an analog-to-digital converter 100 based on the prior art, the n comparators 101 compare the input voltage  $V_{in}$  108 with reference voltages  $V_{ref,i}$  which are generated using the resistor network comprising resistors 105. The resistor network is normally in the form of a linear voltage divider which is used to apply a reference voltage  $V_{ref+}$  or  $V_{ref-}$ . By using the same resistors 105, the reference voltage  $V_{ref}=V_{ref+}-V_{ref-}$  is distributed evenly over the comparators.

Known circuit designs for analog-to-digital converters are based on the "flash" process. In this context, the input voltage  $V_{in}$  108 for digitization is simultaneously applied to the first inputs 102 of the comparators 101.

To achieve a resolution of  $n$  bits,  $2^n - 1$  comparators 101 are required. The second input 103 of the comparators 101 has respective different subvoltages applied to it which are produced using an integrated reference 5 resistor network comprising the resistors 105. The accuracy or the resolution of the analog-to-digital converter 100 is determined essentially by the accuracy of the reference resistor network and by the offset in the comparators 101. These factors are determined by 10 statistical variations in component parameters, which decrease as the surface area of the components increases.

15 The conversion speed of an A/D converter 100 is determined primarily by the architecture and by the speed of the comparators 101. Often, a sample-and-hold circuit is connected upstream of the actual converter block, said sample-and-hold circuit storing and holding the input voltage at a particular time in analog form 20 and making it available to the converter block. This also limits the conversion speed and/or the resolution of the converter.

25 The analog-to-digital converter based on the prior art has a conversion speed which is in need of improvement.

Depending on the model, a comparator has a defined voltage window within which it works in optimum 30 fashion, i.e. it provides the comparison result for its two analog input voltages in a sufficiently short time and with sufficient accuracy at the output 104 in digital form. The signal propagation time in a 35 comparator 101 is always dependent on the input voltage for the comparator 101, however. There is an optimum input voltage at which the comparison result is available in comparatively short time. If the input voltage approaches the limits of the voltage window, the propagation time in a comparator increases and the

conversion speed is reduced.

5 In the case of the analog-to-digital converter 100 based on the prior art, each of the comparators 101 operates at a different input voltage. The comparators 101 therefore need to be designed for a wide input voltage range.

10 Hence, in the case of the described flash architecture based on the prior art, the principle means that a different input voltage is applied to each comparator, which means that each comparator has a different signal propagation time.

15 20 To process differential signals in an analog-to-digital converter, the prior art involves the two mutually antiphase input signals for respective independent comparators being converted into a digital signal and then digitally subtracted. In rare cases, complex comparators having four inputs are even used.

25 [1] discloses an analog-to-digital converter having a first resistor ladder between a first reference voltage and a second reference voltage and also having a second resistor ladder whose two end sections are coupled to an analog signal source.

30 [2] discloses an analog-to-digital converter having a plurality of amplifiers whose inputs are supplied with an analog signal via a resistor chain.

35 [3] discloses an analog-to-digital converter in which the influence of an offset needs to be reduced and A/D conversion needs to take place sufficiently quickly and accurately.

[4] discloses an analog-to-digital converter having two networks of resistor elements to which analog signals

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are applied and which are coupled to inputs on comparators.

[5] discloses an analog-to-digital converter which can  
5 be used to compensate for a comparator offset.

The invention is based on the problem of specifying an analog-to-digital converter which has an increased conversion speed over the prior art.

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The problem is solved by an analog-to-digital converter having the features in line with the independent patent claim.

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The inventive analog-to-digital converter for converting a signal to be digitized into a digitized signal has a plurality of comparators, each of which has a first and a second input and an output, which output can be used to provide the digitized signal. In  
20 addition, the inventive analog-to-digital converter contains an impedance network for each comparator, which is coupled to at least one input of the comparator, where a respective impedance network is connected between the associated comparator and the  
25 signal to be digitized and is connected between the associated comparator and a first electrical reference potential. The impedance networks are set up such that the comparators are brought essentially to the same operating point close to their specific decision  
30 threshold.

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"Close to the specific decision threshold" may mean, in particular, that the operating state of a comparator is chosen or can be set within a prescribed tolerance  
35 range around the decision threshold.

One basic idea of the invention is the use of a resistor network at the input to shift the input

voltages for the comparators in the analog-to-digital converter to almost the same voltage value, i.e. to operate the comparators at the same operating point. This significantly reduces the problems which arise in 5 the prior art with greatly differing signal propagation times in the comparators in an analog-to-digital converter.

10 The inventive analog-to-digital converter clearly uses a resistor network at the converter input to shift the input voltages for the comparators such that all comparators can be operated at approximately the same operating point. The comparator can thus be optimized to this operating point, which means that the analog-15 to-digital converter has an increased conversion speed. The synchronization of the comparator results which is achieved in this manner means that it is additionally possible to dispense with a sample-and-hold circuit as is frequently required in the prior art, which 20 additionally improves the performance of the analog-to-digital converter or reduces the manufacturing complexity.

25 Expressed another way, the resistor network which the invention connects between the signal for digitization and the comparators at the input of the converter replaces the resistor network between the reference voltage and the comparators which is required for producing reference voltages in the case of known flash 30 converters. In line with the invention, it is possible to resort to a greatly simplified comparator architecture, which additionally improves the conversion speed of the converter and simplifies the circuit design in modern CMOS processes at low 35 operating voltages. The approximately identical input voltages for the comparators mean that calibration techniques ("autozeroing" techniques) are also easy to implement for the purpose of reducing offsets in the

comparators which result from manufacture, for example.

In addition, the inventive circuit architecture for the analog-to-digital converter permits genuine rail-to-rail operation of the analog-to-digital converter. That is to say that the analog input voltage for the converter may be between an upper operating voltage limit and a lower operating voltage limit. If the impedance network is provided with suitable dimensions, the input voltage may even exceed/undershoot the operating voltage limits.

CMOS analog-to-digital converters known from the prior art often have a nonreactive input resistance bordering on infinity, which means that a purely capacitive input impedance is provided. In contrast to this, the input of the inventive analog-to-digital converter has an input impedance with a resistive component on account of the use of a resistor network at the input. Particularly in the case of converters with high conversion rates and therefore usually high input frequencies, the resistive component of the input impedance may even be an advantage. At high input frequencies, a terminating resistor for an input line in the form of a waveguide is normally necessary anyway in order to avoid signal reflections. The capacitive load would need to be operated by the source anyway, and the capacitive load has the same order of magnitude as the resistive load at high input frequencies. With the inventive analog-to-digital converter architecture, the terminating resistor is already present in the form of the input resistance of the analog-to-digital converter.

Preferred developments of the invention emerge from the dependent claims.

The second input of at least some of the comparators,

preferably of all comparators, in the inventive analog-to-digital converter may be brought to a second electrical reference potential. The second electrical reference potential may be the ground potential, for  
5 example.

At least some of the impedance networks for the comparators in the analog-to-digital converter may have a first nonreactive resistor and a second nonreactive  
10 resistor, the first nonreactive resistor being connected between the first input of at least some of the comparators and the first electrical reference potential. The second nonreactive resistor may be connected between the first input of at least some of  
15 the comparators and the signal to be digitized.

At least some of the impedance networks may have a voltage divider. The voltage divider may have a first impedance or may be formed thereby, said first  
20 impedance being connected between the first input and a third electrical reference potential. In addition, the voltage divider may have a second impedance or may be formed thereby, said second impedance being connected between the first input and the first electrical  
25 reference potential. The first impedance may be a third nonreactive resistor and/or the second impedance may be a fourth nonreactive resistor. Each of the nonreactive resistors may be produced, by way of example, using one or more nonreactive single resistors. Alternatively,  
30 the first impedance may be a first capacitance and/or the second impedance may be a second capacitance. In other words, the voltage divider may either have a capacitive and/or a resistive component. Each of the capacitances may be produced using one or more  
35 capacitors, for example.

The third electrical reference potential may be the electrical ground potential. Hence, the potential

across the first impedance in the voltage converter may be identical to the electrical potential at the second inputs of the comparators, which means that the number of reference potentials required is kept down.

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The first electrical reference potential may be split into a first potential part and into a second potential part, with a first portion of the comparators having their impedance network connected between the first input and the first potential part, and with a second portion, preferably the remaining portion, of the comparators having their impedance network connected between the first input and the second potential part.

By way of example, the first half of comparators in the inventive analog-to-digital converter may be connected to a positive reference potential as the first potential part, whereas the second portion of the comparators (e.g. the second half of the comparators) may be connected to a negative second potential part.

With an uneven number of  $n$  comparators,  $(n-1)/2$  comparators may be connected to the positive reference potential,  $(n-1)/2$  other comparators may be connected to the negative reference potential, and a comparator may be connected to the positive or to the negative or to another reference potential.

Preferably, the second and/or the third electrical reference potential have a value between the first and the second potential part, their potential preferably being the arithmetic mean from the first and second potential parts. The second and/or the third electrical reference potential may thus be the electrical ground potential, the first potential part may be a potential which is increased by a prescribed value over the ground potential, and the second potential part may be a potential which is reduced by this value.

At least some of the comparators may have a calibration

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device provided for them which is set up such that it can be used to correct a parameter fluctuation between different comparators.

5 As a result of manufacture, the comparators in the analog-to-digital converter may have a different offset value, which fluctuation may impair the functionality of the analog-to-digital converter. The calibration device may be used to compensate for this fluctuation,  
10 which means that a smooth functionality in the analog-to-digital converter is made possible.

By way of example, the calibration device may have a switching element (which may be provided in the form of  
15 a transistor switch, for example) between the first input of a comparator and the impedance network, which switching element can be used to couple the first input of the comparator to the impedance network in a detection mode. Alternatively, the first input may be  
20 brought to a fourth electrical reference potential in a calibration mode, a resultant signal at the output of the comparator in this operating state being taken as a basis for calibrating the comparator using the calibration device.

25 The fourth electrical reference potential may be the same as the second electrical reference potential and may, in particular, be the same as the ground potential. Clearly, the first input and the second  
30 input may be brought to the same electrical potential in the calibration mode and the resultant output signal may be taken as a basis for eliminating or reducing a possible offset in the associated comparator.

35 The value of at least one of the first to fourth nonreactive resistors may be calculated, in at least some of the impedance networks, on the basis of the criterion that one of the first inputs of the

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comparators has a signal applied to it which is essentially the same as the second electrical reference potential. This specific comparator clearly represents that location in the arrangement of comparators at 5 which the outputs of the comparators change from a logic value "1" to a logic value "0" (or vice versa).

The value of the first to fourth nonreactive resistors may additionally or alternatively be calculated, at 10 least for some of the impedance networks, on the basis of the criterion that altering the signal to be digitized by a prescribable value results, for at least some of the comparators, in an alteration to the electrical potential at their first input by an 15 essentially equal value.

Clearly, the values of the resistors are chosen such that the sensitivity of the comparator voltage to the input voltage is essentially the same for all 20 comparators.

In addition, the value of at least one of the first to fourth nonreactive resistors may be calculated, for at least some of the impedance networks, on the basis of 25 the criterion that the nonreactive output resistance of at least some of the impedance networks is essentially the same.

In line with one preferred exemplary embodiment, all 30 three of the criteria described above may be taken as a basis for calculating optimized values of the nonreactive resistors in the impedance networks of the inventive analog-to-digital converter.

35 In addition, in the case of the inventive analog-to-digital converter, at least some of the comparators have the impedance network containing a first impedance device part coupled to the first input and an impedance

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device part coupled to the second input. In addition, the signal to be digitized may be split into a first and into a second signal part to be digitized. The first electrical reference potential may be split into 5 a first potential part and into a second potential part. The impedance device part may be connected between the first input, the first signal part for digitization and the first potential part. The second impedance device part may be connected between the 10 second input, the second signal part to be digitized and the second potential part.

The first and second signal parts for digitization may 15 be differential signals.

In other words, the inventive analog-to-digital converter may, in particular, also match circuit architectures in which an input signal to be digitized is provided in duplicate, i.e. in the form of two 20 complementary signals. In such a case, the first input of the comparator receives one of the two differential signals to be digitized which have been modified by means of the impedance network, and the second input receives the other of the two differential signals to 25 be digitized, again modified by means of the impedance network.

In the case of the inventive analog-to-digital converter, the first impedance device part may have a 30 first nonreactive resistor and a second nonreactive resistor, the first nonreactive resistor being connected between the first input and the first electrical potential part, the second nonreactive resistor being connected between the first input and the first signal part to be digitized. In addition, the second impedance device part may have a third nonreactive resistor and a fourth nonreactive resistor, 35 the third nonreactive resistor being connected between

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the second input and the second electrical potential part, and the fourth nonreactive resistor being connected between the second input and the second signal part to be digitized. Clearly, the two signal  
5 paths for the differential signals are designed such that they mirror one another.

At least one fifth nonreactive resistor may be connected between the first and second inputs. The  
10 fifth nonreactive resistor may be a single resistor, for example, or may be split into two resistor parts.

The fifth nonreactive resistor may be split into a first and into a second resistor part, with a  
15 connection between the first and second resistor parts being able to be brought to a fifth electrical reference potential, preferably to the electrical ground potential. In line with this refinement, a center tap is provided between the two resistor parts  
20 and may be brought to a defined electrical potential.

The analog-to-digital converter of the invention may be set up as an integrated circuit, and in particular may be integrated on and/or in a substrate, preferably a  
25 semiconductor substrate (e.g. using silicon technology).

Exemplary embodiments of the invention are shown in the figures and are explained in more detail below.

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In the figures:

figure 1 shows an analog-to-digital converter based on the prior art,

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figure 2 shows an analog-to-digital converter based on a first exemplary embodiment of the invention,

figure 3 shows an analog-to-digital converter based on a second exemplary embodiment of the invention,

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figure 4 shows an analog-to-digital converter based on a third exemplary embodiment of the invention,

10 figure 5 shows an analog-to-digital converter based on a fourth exemplary embodiment of the invention,

15 figures 6A and 6B show tables for resistor values for the inventive analog-to-digital converter,

20 figure 7 shows an analog-to-digital converter based on a fifth exemplary embodiment of the invention,

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figure 8 shows an analog-to-digital converter based on a sixth exemplary embodiment of the invention.

25 The same or similar components in different figures have been provided with the same reference numerals.

The illustrations in the figures are schematic and not to scale.

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The text below describes an analog-to-digital converter 200 based on a first exemplary embodiment of the invention with reference to figure 2.

35 The analog-to-digital converter 200 contains a multiplicity of comparators 201, each of which has a first input 202, a second input 203 and an output 204. The output 204 of each of the comparators 201 provides

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1 bit of a thermometer code which represents the digitized signal. Put another way, each output 204 of each comparator 201 provides a signal having a first logic value (e.g. logic value "1") or having a second logic value (e.g. logic value "0"), on the basis of which electrical potentials are applied to the inputs 202, 203 of the respective comparator 201. In addition, each comparator 201 is provided with a resistor network 212 comprising first to third nonreactive resistors 209 to 211, which is coupled to the first input 202 of each comparator 201. The resistor network 212 associated with the respective comparator 201 is connected between the associated comparator 201 and a signal  $V_{in}$  207 to be digitized. In addition, the resistor network 212 is connected between an associated comparator 201 and an associated electrical reference potential  $V_{ref+}$  205 or  $V_{ref-}$  206. The analog-to-digital converter 200 has n comparators 201. The upper portion of comparators 201 in figure 2 has a positive reference potential  $V_{ref+}$  as electrical reference potential, whereas the lower portion of the comparators 201 in figure 2 has a negative reference potential 206  $V_{ref-}$  as electrical reference potential. The second input 203 of the comparators 201 has respectively been brought to the electrical ground potential 208. The first nonreactive resistor 209  $R_{ref,i}$  is connected between the respective reference potential 205 or 206, on the one hand, and the first input 202 of the associated comparator 201. The second nonreactive resistor  $R_{in,i}$  of a respective comparator 201 is connected between the first input 202 of the associated comparator 201 and the signal  $V_{in}$  207 to be digitized. In addition, a third nonreactive resistor  $R_{gnd,i}$  211 is connected between the first input 202 of the associated comparator 201 and the electrical ground potential 208.

The analog-to-digital converter 200 contains n comparators, where n is preferably an uneven number. As

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figure 2 shows, the electrical potential  $V_{ref+}$  is applied to those first nonreactive resistors 209 which are associated with the upper  $(n-1)/2$  comparators 201 in figure 2. The electrical potential  $V_{ref-}$  is applied 5 to those first nonreactive resistors 209 which are associated with the lower  $(n-1)/2$  comparators 201 in figure 2. That comparator 201 which is arranged between the  $(n-1)/2$  upper and the  $(n-1)/2$  lower comparators 201, namely the comparator 201 with the index "0", is 10 not provided with a first nonreactive resistor 209. Put in clear terms, a nonreactive resistor 209 could also be provided for the comparator 201 with the index "0"; this comparator would then have a nonreactive resistor value approaching infinity.

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It should be noted that the values of the first nonreactive resistor  $R_{ref,i}$  209 may be different for different comparators 201. Similarly, the values of the second and third nonreactive resistors  $R_{in,i}$  210,  $R_{gnd,i}$  211 from different comparators 201 may have different 20 values.

The text below describes the functionality of the 25 analog-to-digital converter 200.

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The input voltage  $V_{in}$  207 is shifted by means of a resistor network 212 connected upstream of each 30 comparator 201 such that an input voltage close to the electrical ground potential 208 is applied close to the specific decision threshold of the respective comparator 201. Hence, all comparators 201 operate at similar operating points and may thus be optimized to the maximum performance. The nonreactive resistors 209 to 211 have the function of shifting the input signal 35  $V_{in}$  207 using the reference voltage  $V_{ref}$  (which is subsequently used as generic term for the positive reference potential 205  $V_{ref+}$  and for the negative reference potential 206  $V_{ref-}$ ) to an extent which is

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such that at a prescribed input voltage  $V_{in,i}$  207 a potential close to the electrical ground potential 208 is applied to a first input 202 on a respective comparator 201. The third nonreactive resistor  $R_{gnd}$  211 5 is used to adapt the sensitivity of a respective comparator 201 for the input voltage  $V_{in,i}$  207.

The following applies for the input node  $V_{comp}$  213 of the i-th comparator 201:

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$$\frac{V_{in} - V_{comp,i}}{R_{in,i}} - \frac{V_{comp,i}}{R_{gnd,i}} + \frac{V_{ref,\pm} - V_{comp,i}}{R_{ref,i}} = 0 \quad (1)$$

To shift the input voltage  $V_{in}$  207 to ground level 208, a reference voltage  $V_{ref,\pm}$  205, 206 is required. This reference voltage is positive ( $V_{ref+}$ ) when a negative 15 input voltage  $V_{in}$  207 is intended to be processed, and is negative ( $V_{ref-}$ ) when a positive input voltage  $V_{in}$  207 is intended to be processed.

20 In line with the exemplary embodiment described, the first secondary condition for calculating the values of the first to third resistors 209 to 211 is that  $V_{comp,i}=0$  for  $V_{in,i}=i \cdot \Delta V$  with  $i=-m, \dots, 0, \dots, +m$ , where  $2m+1=n$ . Clearly, this means that the input voltage  $V_{comp,i}$  on the i-th comparator 201 needs to be exactly zero when the 25 input voltage 207 has a particular value  $V_{in,i}=i \cdot \Delta V$ .

This is expressed by equation (2):

$$\frac{i \cdot \Delta V}{R_{in,i}} + \frac{V_{ref,\pm}}{R_{ref,i}} = 0 \quad (2)$$

30 In equation (2)  $\Delta V$  denotes a (sufficiently small) voltage difference which corresponds to the least significant bit (LSB) in the analog-to-digital converter 200 and thus determines the resolution.

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The second secondary condition demanded for calculating the values of the nonreactive resistors 209 to 211 is that the sensitivity of the comparator voltage to the input voltage be the same for all comparators 201. When 5 the input voltage changes by  $\Delta V_{in}$ , for example, the input voltage on each comparator 201 close to its decision threshold  $V_{comp,i}=0$  needs to change by a value  $\Delta V_{comp}$ :

$$\frac{\partial V_{comp,i}}{\partial V_{in}} = \frac{1}{1 + \frac{R_{in,i}}{R_{ref,i}} + \frac{R_{in,i}}{R_{gnd,i}}} = \text{const.} \quad \forall i \quad (3)$$

10

To keep the influence of parameter fluctuations at a low level, this value needs to be as large as possible. Within the n comparators 201 in the analog-to-digital converter 200, the two comparators 201 with  $i=-m$  and 15  $i=+m$  have the least sensitivity.

In addition, signal dynamics considerations allow a third secondary condition to be formulated for calculating the values of the nonreactive resistors 209 20 to 211. Since each comparator input has an input capacitance, a low-pass filter is clearly formed in combination with the upstream resistor network 212. So that the input signal undergoes essentially the same frequency shaping on each comparator 201, the output 25 resistance  $R_{out}$  of the resistor network 212 should be identical for all comparators 201:

$$\frac{1}{R_{in,i}} + \frac{1}{R_{ref,i}} + \frac{1}{R_{gnd,i}} = \frac{1}{R_{out}} = \text{const.} \quad \forall i \quad (4)$$

30 Calculating the resistor values 209 to 211 is particularly simple when the positive reference voltage  $V_{ref+}$  205 or the negative reference voltage  $V_{ref-}$  corresponds to the limit values of the input voltage  $V_{in}$  207, i.e.  $V_{ref+}=m \cdot \Delta V$  or  $V_{ref-}=-m \cdot \Delta V$ .

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In this case, it follows directly from equation (2) that  $R_{in,m}=R_{ref,m}$ . In addition, it follows from (3):

$$\frac{\partial V_{comp,m}}{\partial V_{in}} = \frac{1}{1 + \frac{R_{in,m}}{R_{ref,m}} + \frac{R_{in,m}}{R_{gnd,m}}} = \frac{1}{2} \quad \text{for } R_{gnd,m} \rightarrow \infty \quad (5)$$

5 This also means that the following applies for all comparators 201:

$$\frac{1}{R_{in,i}} = \frac{1}{R_{ref,i}} + \frac{1}{R_{gnd,i}} \quad (6)$$

Using (4), it thus follows:

10

$$R_{in,i} = 2R_{out} = R_{in} = \text{const.} \quad \forall i \quad (7)$$

The second resistor  $R_{in}$  210 in all resistor networks 212 has the same value in this case.

15 To calculate all resistor values 209 to 211 unambiguously, it is expedient to determine the input resistance for the whole converter 200. This will be  $50\Omega$ , for example, which is a normal impedance in radio-frequency engineering. If a 6-bit analog-to-digital converter 200 is to be produced, at least 63 comparators need to be connected in parallel with their respective input resistor networks 212. To simplify calculation, it is subsequently assumed that 64 resistor networks 212 are connected in parallel. In 20 this case, the input resistance of a single network is 3200 $\Omega$ , and it follows from  $R_{in,m}=R_{ref,m}$  that  $R_{in}=R_{ref,m}=1600\Omega$ . The value of  $R_{ref,i}$  can be calculated from equation (2), and the value  $R_{gnd,i}$  can be calculated from equation (5).

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Hence, all resistances 209 to 211 have been clearly determined and the inventive resistor network 212 will condition the input voltage for the analog-to-digital

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converter 200 for each comparator 201 such that all comparators 201 are always operated at an optimum operating point.

5 Figure 6A shows the resistor values 209 to 211 for a 6-bit converter having an input impedance of  $50\Omega$  and for the exemplary embodiment shown in figure 2 (in  $\Omega$ ).

10 It should be noted that the third nonreactive resistors  $R_{gnd,i}$  211 are optional and may also be omitted in order to obtain an analog-to-digital converter which can be produced with even less complexity. When using the third nonreactive resistors  $R_{gnd}$  211, however, there is the assurance that the comparators 201 are operated at 15 approximately the same sensitivity, which results in an increased effective resolution for the converter 200.

20 The text below makes reference to figure 3 to describe an analog-to-digital converter 300 based on a second exemplary embodiment of the invention.

The analog-to-digital converter 300 differs from the analog-to-digital converter 200 essentially by virtue of the modified interconnection of nonreactive 25 resistors in the resistor networks. The analog-to-digital converter 300 has first nonreactive resistors 301, second nonreactive resistors 302 and third nonreactive resistors 303. The third nonreactive resistors 303 in figure 3 have essentially the same 30 function as the third nonreactive resistors 211 in figure 2. By contrast, the functionality of the first and second nonreactive resistors 301, 302 in the analog-to-digital converter 300 is not identical to the functionality of the first and second resistors 209, 35 210 from figure 2.

If one considers the top left-hand comparator 201 in figure 3, for example, its second input 203 is again

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grounded, i.e. has been brought to the electrical ground potential 208. Connected between the first input 202 of the comparator 201 under consideration and the ground potential 208 is a third nonreactive resistor  $R_{b1}$  303. In addition, the first input 202 and the signal  $V_{in}$  207 to be digitized have a nonreactive total resistance connected between them which is made up of the first nonreactive resistor 301  $R_{a1}$  and the second nonreactive resistor  $R_1$  302. The resistors  $R_{a1}$  and  $R_1$  clearly form an effective total resistance which is comparable to the resistor  $R_{in,i}$  210 from figure 2. In addition, the first input 202 of the comparator 201 and the positive reference potential  $V_{ref+}$  205 have a chain of resistors connected between them which is formed from the first resistor 301  $R_{a1}$  and a multiplicity of second resistors 302 ( $R_2$ ,  $R_3$ , ...,  $R_m$ ,  $R_{ref}$ ). The functionality of the resistors  $R_{a1}$ ,  $R_2$ ,  $R_3$ , ...,  $R_m$ ,  $R_{ref}$  is comparable to the functionality of the first nonreactive resistor  $R_{ref,i}$  209 from figure 2.

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In line with figure 3, the input voltage  $V_{in}$  207 is applied to a reference resistor network which generates input voltages for the comparators 201. The respective second input 203 of the comparators 201 is at the electrical ground potential 208. Each comparator 201 operates approximately at the same input voltage value and hence at almost the same operating point. In addition, the sensitivity of the comparators 201 is approximately identical as a result of a suitable choice of single resistors 301 to 303 for all comparators 201.

35 Clearly, the input voltage  $V_{in}$  207 is divided or shifted using a series-path resistor chain comprising the second resistors  $R_i$  302. Using the first resistors  $R_{a,i}$  301 and the second resistors  $R_{b,i}$  302, it is possible to set the sensitivity of the individual comparators 201. The resistor values for the nonreactive resistors 301

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to 303 cannot be calculated analytically in the case of the analog-to-digital converter 300. For this reason, the values of the nonreactive resistors 301 to 303 are ascertained by solving the following equation system numerically:

$$\frac{V_{i-1} - V_i}{R_i} + \frac{V_{i+1} - V_i}{R_{i+1}} - \frac{V_i}{R_{ai} + R_{bi}} = 0 \quad (8)$$

and

$$\frac{V_{comp,i}}{V_i} = \frac{R_{bi}}{R_{ai} + R_{bi}} \quad (9)$$

with the secondary conditions:

$$V_{comp,i} = 0 \text{ for } V_{in,i} = i \cdot \Delta V \text{ with } i = -m, \dots, 0, \dots, m \quad (2m + 1 = n) \quad (10)$$

and

15

$$\frac{\partial V_{comp,i}}{\partial V_{in}} = \text{const.} \quad \forall i \quad (11)$$

On account of the many degrees of freedom for the numerical calculation, it is also possible to take into account further secondary conditions such as the output 20 resistance of the network on the comparator connections.

The text below makes reference to figure 4 to describe an analog-to-digital converter 400 based on a third 25 exemplary embodiment of the invention.

The analog-to-digital converter 400 differs from the analog-to-digital converter 300 shown in figure 3 essentially by virtue of the first and third 30 nonreactive resistors 301, 303 having been omitted.

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Consequently, the comparators 201 in the analog-to-digital converter 400 may have slightly different sensitivities. However, the resistor network from figure 4 is greatly simplified over that in figure 3, 5 and progressive analytical calculation of the values of the resistors 302 is possible.

For the voltage  $V_{comp,i}$  at the nodes 401 which are coupled to the first input 202 of the comparators 201, 10 the following applies generally:

$$\frac{V_{in} - V_{comp,i}}{\sum_{j=1}^i R_j} + \frac{V_{ref,t} - V_{comp,i}}{\sum_{j=i+1}^m R_j + R_{ref}} = 0 \quad (12)$$

A secondary condition for calculating the resistor values 302 is  $V_{comp,i}=0$  for  $V_{in,i}=i \cdot \Delta V$  with 15  $i=-m, \dots, 0, \dots, +m$ , where  $2m+1=n$ . Clearly, this means that the input voltage on the  $i$ -th comparator  $V_{comp,i}$  needs to be exactly 0 when the input voltage has a particular value  $V_{in,i}=i \cdot \Delta V$ .

20 It thus follows from (12):

$$\frac{i \cdot \Delta V}{\sum_{j=1}^i R_j} + \frac{V_{ref,t}}{\sum_{j=i+1}^m R_j + R_{ref}} = 0 \quad (13)$$

$\Delta V$  will be a small voltage difference which corresponds to the least significant bit (LSB) in the analog-to-digital converter 400. Simple calculation of the resistor values 302 is possible under the assumption that the reference potential  $V_{ref}$  corresponds to the negative maximum input voltage for the analog-to-digital converter 400 ( $V_{ref+}=m \cdot \Delta V$ ,  $V_{ref-}=-m \cdot \Delta V$ ). In this 25 case, it holds true that  $\sum_{j=1}^m R_j = R_{ref}$ , and it follows 30 from (13):

$$\frac{i \cdot V_{ref,\pm}}{\frac{1}{m} \sum_{j=1}^i R_j} = \frac{V_{ref,\pm}}{2R_{ref} - \sum_{j=1}^i R_j} \quad (14)$$

This can be simplified further to give:

5

$$R_i = \frac{2R_{ref}}{\frac{m}{i} + 1} - \sum_{j=1}^{i-1} R_j \quad (15)$$

In this case, the input resistance of the resistor network comprising the resistors 302 is obtained as  $R_{in}=2R_{ref}/2=R_{ref}$ . This value is obtained from the parallel 10 connection of two networks (positive and negative paths) with a nonreactive resistor of  $2R_{ref}$  in each case. If an input resistance of  $50\Omega$  is to be provided again, then  $R_{ref}=50\Omega$  needs to be chosen accordingly.

15 Using this choice of resistor value, formula (15) can be used to calculate the values of all further resistors progressively, starting at  $R_1$ .

Figure 6B shows the resistor values (in  $\Omega$ ) for a 6-bit 20 converter based on the exemplary embodiment from figure 4.

If the value of the input resistance is chosen too high, dynamic distortions may arise during converter 25 operation. In this case, the chain comprising resistors 302 and the input capacitances of the comparators 201 acts as a low-pass filter, which means that the comparators 201 with a high ordinal number, hence the  $m$ -th comparator, in particular, receive a slightly 30 phase-shifted input signal. This is avoided in the case of the analog-to-digital converter 200 shown in figure 2.

The text below makes reference to figure 5 to describe an analog-to-digital converter 500 based on a fourth exemplary embodiment of the invention.

5

To be more precise, figure 5 shows the interconnection of a comparator 201 in an analog-to-digital converter using a calibration device 501. Hence, an analog-to-digital converter having a plurality of comparators can 10 be formed from the interconnection of the comparator 201 from figure 5 in a similar manner to that shown in figure 2 or figure 3 or figure 4.

15 The single stage of an analog-to-digital converter 500 which is shown in figure 5 differs from a single stage in the analog-to-digital converter 200 from figure 2 essentially by virtue of a calibration device 501 and a switch 502 being provided. The switch element 502 can be used to couple the first input 202 of the comparator 20 201 to the resistor network 212 in a measurement mode (see the switch position shown in figure 5 for the switch 502).

25 In the position of the switch 502 which is complementary to that in figure 5, the first input 202 has been brought to the electrical ground potential 208. In this position, the two inputs 202, 203 of the comparator 201 are at the electrical ground potential 208. On the basis of an output signal (ascertained in 30 this scenario) from the comparator 201 at its output 204, the calibration device 501 for which this output signal has been provided readjusts the comparator 201 such that a possible offset in the comparator is equalized thereby.

35

Comparators 201 may have discrepancies in the position of their decision threshold on account of physical effects. In a comparator 201 which compares two

voltages with one another, this is expressed in the form of an input voltage offset. These offset voltages are evenly distributed and are dependent on the characteristics of the semiconductor process for 5 producing the comparators 201 and on the surface areas of all of the components used in the comparator 201. In this case, it holds true that the statistical discrepancy in the input voltage decreases as component surface area increases. When using very small-area 10 components, this effect may result in the monotonicity of the digital signals no longer being assured. If the offset in a comparator 201 is greater than the voltage margin  $\Delta V$  of the switching threshold, a situation may arise in which at a particular input voltage a more 15 significant comparator 201 is already indicating an output value with a logic value "1" and simultaneously a less significant comparator 201 is indicating an output value with a logic value "0" (or vice versa). The thermometer code provided at the output of the 20 comparators 201 is therefore interrupted, which means that complex correction may be necessary in a downstream digital logic unit. In addition, an offset voltage in the comparators results in a reduction in the effective resolution of the converter. For these 25 reasons, either the offset in the comparators needs to be chosen to be sufficiently low (which results in restrictive conditions for the component surface areas) and/or a calibration device like the calibration device 501 shown in figure 5 may be provided.

30

Since the invention has the decision threshold of all comparators 201 at an input voltage close to the ground potential 208, the comparators 201 may be calibrated particularly easily by applying the ground potential 35 201 to the first input 202. This is implemented in figure 5 by means of the switch 502 (semiconductor switch/transmission gate), which changes over the input 202 of the comparator 201 between the input voltage

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$V_{comp,i}$  and the ground voltage 208. In a defined input state, the calibration device 501 can adjust the comparator 201 such that it is exactly at the labile operating point. This adjustment is stored, and the 5 comparator 201 can be operated in the measurement mode again. In contrast to conventional analog-to-digital converters, a multiplicity of additional calibration voltages are thus not necessary in order to calibrate the inventive analog-to-digital converter 500, it 10 merely being necessary to apply the ground potential 208, which is available anyway, to the first input 202 of the comparators 201.

15 It should be noted that a calibration circuit such as the one shown in figure 5 can be included in any other exemplary embodiment of an analog-to-digital converter based on the invention.

20 In the case of the calibration device in the inventive analog-to-digital converter 500, very simple offset correction thus takes place in the comparators 201, since they are operating approximately at the same value of the input voltage. Each first comparator input 202 is applied to ground potential 208 by means of the 25 switch 502, the comparison result at the output 204 is evaluated and the comparator 201 is trimmed using an adjustment input 503 which is accessed by the calibration device 501.

30 The text below makes reference to figure 7 and figure 8 to describe two additional exemplary embodiments of inventive analog-to-digital converters which are set up to process a differential input signal.

35 Particularly in radio-frequency engineering, an input signal is frequently available in the form of a differential signal. Two mutually antiphase input signals  $V_{in+}$  and  $V_{in-}$  are frequently converted into a

digital signal by respective independent comparators in an analog-to-digital converter based on the prior art and are then digitally subtracted.

5 The inventive analog-to-digital converters 700, 800 shown in figure 7 and figure 8 are particularly well suited to the processing of differential signals. To this end, as a departure from the exemplary embodiments from figure 2 to figure 4, a shifted voltage signal 10  $V_{comp,i+}$  from the positive path and the signal  $V_{comp,i-}$  from the negative path are respectively applied to the two inputs of a respective comparator 201. If the input voltage passes the voltage value provided for this resistor network, then one input voltage for the 15 comparator passes the ground potential in the positive direction and the other input voltage passes it in the negative direction. As a result of this architecture, the effective voltage swing on the comparator is twice as high as in the case of the nondifferential 20 architecture. The doubled input amplitude on the comparator causes a reduction in the demands on the input voltage offset for the comparators accordingly. The differential signal processing may be implemented in any of the exemplary embodiments already presented.

25

The text below makes reference to figure 7 to describe an analog-to-digital converter 700 based on a fifth exemplary embodiment of the invention.

30 Again, figure 7 shows just one stage, i.e. a comparator and an associated resistor network, of an analog-to-digital converter 700. The analog-to-digital converter 700 shown in figure 7 has a total of n such stages.

35 The analog-to-digital converter 700 from figure 7 again has a comparator 201 with a first input 202 and a second input 203, and also with an output 204. Connected between the second input 203 and the positive

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reference signal  $V_{ref+}$  205 is a first nonreactive resistor 701  $R_{ref,(n-1)/2}$ . Connected between the first input 202 and the negative reference potential  $V_{ref-}$  206 is a second nonreactive resistor  $R_{ref,-(n-1)/2}$ . In 5 addition, the second input 203 and a first signal part 706  $V_{in+}$  for digitization have a third nonreactive resistor  $R_{in,(n-1)/2}$  connected between them. The second input 203 and a first signal part 706 for digitization have a third nonreactive resistor  $R_{in,(n-1)/2}$  703 10 connected between them. The first input 202 and a second signal part 707 for digitization have a fourth nonreactive resistor  $R_{in,-(n-1)/2}$  704 connected between them. In addition, the first and second inputs 202, 203 have a fifth nonreactive resistor  $2R_{gnd,(n-1)/2}$  705 15 connected between them. The fifth nonreactive resistor may also be split into two resistor parts whose center tap can be brought to a reference potential (e.g. the electrical ground potential). The signal parts 706, 707 form a differential input signal which is processed 20 jointly by the comparator 201. The stage in the analog-to-digital converter 700 which is shown in figure 7 represents the analog for the top stage shown in figure 2. Resistors 701 to 705 form a resistor network 708.

25 The differential input voltages  $V_{in+}$  706 and  $V_{in-}$  707 are shifted by means of two resistor dividers, which are connected upstream of each of the total of n comparators 201, such that all comparators 201 may operate essentially at the same operating point.

30 The text below makes reference to figure 8 to describe an analog-to-digital converter 800 based on a sixth exemplary embodiment of the invention.

35 Analog-to-digital converter 800 is set up to process a differential input signal 706, 707. The nonreactive resistors 801 in figure 8 replace the nonreactive resistors 701 to 705 from figure 7. Clearly, the

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differential input voltages  $V_{in+}$  and  $V_{in-}$  706, 707 shown in figure 8 are shifted by means of two resistor networks (the top chain of nonreactive resistors 801 shown in figure 8 or the bottom chain of nonreactive resistors 801 shown in figure 8) such that all comparators 201 operate essentially at the same operating point.

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## List of reference numerals

- 100 Analog-to-digital converter
- 101 Comparators
- 5 102 First input
- 103 Second input
- 104 Output
- 105 Nonreactive resistors
- 106 Positive reference potential
- 10 107 Negative reference potential
- 108 Signal to be digitized
- 200 Analog-to-digital converter
- 201 Comparators
- 202 First input
- 15 203 Second input
- 204 Output
- 205 Positive reference potential
- 206 Negative reference potential
- 207 Signal to be digitized
- 20 208 Ground potential
- 209 First nonreactive resistor
- 210 Second nonreactive resistor
- 211 Third nonreactive resistor
- 212 Resistor network
- 25 213 Input node
- 300 Analog-to-digital converter
- 301 First nonreactive resistor
- 302 Second nonreactive resistor
- 303 Third nonreactive resistor
- 30 400 Analog-to-digital converter
- 401 Node
- 500 Analog-to-digital converter
- 501 Calibration device
- 502 Switch
- 35 503 Adjustment input
- 700 Analog-to-digital converter
- 701 First nonreactive resistor
- 702 Second nonreactive resistor

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- 703 Third nonreactive resistor
- 704 Fourth nonreactive resistor
- 705 Fifth nonreactive resistor
- 706 First signal part for digitization
- 5 707 Second signal part for digitization
- 708 Resistor network
- 800 Analog-to-digital converter
- 801 Nonreactive resistors